23.4 A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link

Noriyuki Miura[1], Daisuke Mizoguchi[1], Mari Inoue[1], Kiichi Niitsu[1], Yoshihiro Nakagawa[2], Masamoto Tago[2], Muneo Fukaishi[2], Takayasu Sakurai[3], Tadahiro Kuroda[1]

[1]Keio University, Yokohama, Japan
[2]NEC Corporation, Sagamihara, Japan
[3]University of Tokyo, Tokyo, Japan

This paper presents a 1Tb/s 3W inter-chip transceiver. The data rate is the highest and the power dissipation is the lowest among transceiver chips reported previously at ISSCC (Fig. 23.4.1). Both clock and data are transmitted by inductive coupling. The clock frequency is 1GHz and data rate per channel is 1Gb/s. 1024 data transceivers are arranged with a pitch of 30μm. The total layout area for the clock and data transceivers is 2mm^2 in 0.18μm CMOS and the chip thickness is 10μm. Time Division Multiple Access (TDMA) using 4 phases reduces crosstalk effectively. The measured Bit Error Rate (BER) is lower than 10^{-12}. Bi-Phase Modulation (BPM) is employed to improve noise immunity, resulting in reduced power dissipation in the transceiver.

The block diagram of the transceiver chip is shown in Fig. 23.4.2. The transceiver comprises 16 slices of transceiver blocks, each of which consists of one clock transceiver and 64 data transceivers. The transmitter clock, *Txclk*, is transmitted to the receiver by inductive coupling. Phase timing of the received clock, *Rxclk*, is adjusted by a delay controller by UI/128 steps. A Phase Interpolator (PI) generates 4-phase clocks for TDMA. A TDMA controller changes the number of phases and phase assignment. A pitch controller selects activated channels to change the channel pitch and the number of aggregated channels. For BER measurement, a Built-In-Self-Test (BIST) circuit is implemented. A Pseudo Random Bit Sequence (PRBS) generator with 23b Linear Feedback Shift Registers (LFSRs) produces a 2^{23}-1 word pattern for transmitting data, *Txdata*. The number of errors in the received data, *Rxdata*, is counted in the receiver.

BPM signaling is employed for the data link. An H-bridge circuit in the data transmitter generates a positive or negative pulse current, I_T, according to *Txdata* in every clock cycle. A Sense-Amplifier Flip-Flop (SAFF) in the data receiver receives the positive or negative pulse voltage, V_R, corresponding to the polarity of I_T, and recovers *Rxdata*. Compared to Non-Return-to-Zero (NRZ) signaling [1, 2] where no signal is transmitted when the same data continues, the noise immunity of the receiver is improved, since the V_R signal is always generated in every clock cycle. Therefore, receiver sensitivity for BPM signaling can be set high enough to detect a 40mV-peak signal while that for NRZ signaling needs to be set low enough to ignore a 120mV-peak signal. The high sensitivity of the receiver for BPM signaling yields larger timing margins and lower BER with smaller transmit power. The transmit power is reduced to 5mA-peak for BPM signaling from 15mA-peak for NRZ signaling. Although switching activity increases for BPM signaling, the overall power dissipation of the transceiver is reduced.

A micrograph of the test chips is shown in Fig. 23.4.3. They are fabricated in 0.18μm CMOS. The transmitter chip is placed on top of the receiver chip, with both chips face up. Both chips are polished to 10μm thickness. Communication distance between the transmitter and the receiver is 15μm, including an adhesive layer. The two chips are aligned by conventional infra-red alignment. The alignment error is less than 3μm. The clock transceiver transmits a 1GHz clock by a metal inductor with a diameter of 200μm. The clock transceiver is set up for every 64 data transceivers. The data transceiver communicates at 1Gb/s/ch by a metal inductor with a diameter of 29μm. 1024 data transceivers are arranged with a pitch of 30μm. The transmitter and receiver circuits are placed under the metal inductors to save layout area. Influence from the transceiver circuits to the inductive channel is negligibly small, which will be shown through experimental results later. The stacked chips are mounted on a wafer, placed on a probe station without an electromagnetic shield, and tested in a laboratory room with no control of temperature, dust or air. A differential clock of 1GHz is provided to the transmitter chip through AC probes. Power and ground are provided by DC probes.

Measurement results of the clock transceiver are depicted in Fig. 23.4.4. A 1GHz clock is successfully transmitted with a peak-to-peak jitter of 80ps in *Rxclk*, some of which is caused by 50ps of jitter in *Txclk* supplied by an external clock generator. The clock transmitter consumes 6.5mW and the clock receiver consumes 6mW from a 1.8V supply.

The measured timing bathtub curve is depicted in Fig. 23.4.5. A BER of less than 10^{-12} is established by the 2^{23}-1 PRBS data of 1Gb/s. With a measured timing margin of 200ps, the timing margin is sufficiently wide that a Clock and Data Recovery (CDR) circuit is not required. A snapshot of data waveforms is also presented in Fig. 23.4.5. The delay time between *Txdata* and *Rxdata* is 10ns, including the delay caused by cable and buffers in the experimental setup. By taking them out, it is confirmed that latency between *Txdata* and *Rxdata* is 1 clock. The data transmitter consumes 2.2mW and the data receiver consumes 0.6mW from a 1.8V supply.

The BER dependence on channel pitch and the number of phases in TDMA was examined and the measured results are plotted in Fig. 23.4.6. By increasing the number of phases in TDMA, crosstalk is reduced and the channel pitch can be shortened for the same BER. 1024 transceivers that are placed with a pitch of 30μm operate at BER of less than 10^{-12} with the 4-phase TDMA. As a result, an aggregate data bandwidth of 1Tb/s is achieved with 2mm^2 area for the clock and data transceivers. The chip consumes 3W at 1Tb/s, which yields an efficiency of 3mW/Gb/s or 3pJ/b. The chip performance is summarized in Fig. 23.4.7.

Acknowledgments:
The VLSI chips in this study have been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with MOSIS and Taiwan Semiconductor Manufacturing Company (TSMC).

References:
[1] D. Mizoguchi et. al., "A 1.2Gb/s/pin Wireless Superconnect based on Inductive Inter-Chip Signaling (IIS)," *ISSCC Dig. Tech. Papers*, pp. 142-143, Feb., 2004.
[2] N. Miura et. al., "A 195Gb/s 1.2W 3D-Stacked Inductive Inter-Chip Wireless Superconnect with Transmit Power Control Scheme," *ISSCC Dig. Tech. Papers*, pp. 264-265, Feb., 2005.
[3] Y. Unekawa et al., "A 5Gb/s 8×8 ATM Switch Element CMOS LSI Supporting Five Quality-of-Service Classes with 200MHz LVDS Interface," *ISSCC Dig. Tech. Papers*, pp. 118-119, Feb., 1996.
[4] Y. Ohtomo et al., "A 40Gb/s 8×8 ATM Switch LSI using 0.25μm CMOS/SIMOX," *ISSCC Dig. Tech. Papers*, pp. 154-155, Feb., 1997.
[5] B. Lau et al., "A 2.6GB/s Multi-Purpose Chip-to-Chip Interface," *ISSCC Dig. Tech. Papers*, pp. 162-163, Feb., 1998.
[6] T. Takahashi et al., "110GB/s Simultaneous Bi-Directional Transceiver Logic Synchronized with a System Clock," *ISSCC Dig. Tech. Papers*, pp. 176-177, Feb., 1999.
[7] M. Fukaishi et al., "A 20Gb/s CMOS Multi-Channel Transmitter and Receiver Chip Set for Ultra-High Resolution Digital Display," *ISSCC Dig. Tech. Papers*, pp. 260-261, Feb., 2000.
[8] K. Yang et al., "A Scalable 32Gb/s Parallel Data Transceiver with On-Chip Timing Calibration Circuits," *ISSCC Dig. Tech. Papers*, pp. 258-259, Feb., 2000.
[9] T. Tanahashi et al., "A 2Gb/s 21CH Low-Latency Transceiver Circuit for Inter-Processor Communication," *ISSCC Dig. Tech. Papers*, pp. 60-61, Feb., 2001.
[10] R. Nair et al., "A 28.5GB/s CMOS Non-Blocking Router for Terabit/s Connectivity between Multiple Processors and Peripheral I/O Nodes," *ISSCC Dig. Tech. Papers*, pp. 224-225, Feb., 2001.
[11] P. Landman et al., "A 62Gb/s Backplane Interconnect ASIC based on 3.1Gb/s Serial-Link Technology," *ISSCC Dig. Tech. Papers*, pp. 52-53, Feb. 2002.
[12] K. Tanaka et al., "A 100Gb/s Transceiver with GND-VDD Common-Mode Receiver and Flexible Multi-Channel Aligner," *ISSCC Dig. Tech. Papers*, pp. 264-265, Feb., 2002.
[13] T. Ezaki et al., "A 160Gb/s Interface Design Configuration for Multichip LSI," *ISSCC Dig. Tech. Papers*, pp. 140-141, Feb., 2004.
[14] G. Paul et al., "A Scalable 160Gb/s Switch Fabric Processor with 320Gb/s Memory Bandwidth," *ISSCC Dig. Tech. Papers*, pp. 410-411, Feb., 2004.
[15] K. Chang et al., "Clocking and Circuit Design for a Parallel I/O on a First-Generation CELL Processor," *ISSCC Dig. Tech. Papers*, pp. 526-527, Feb., 2005.

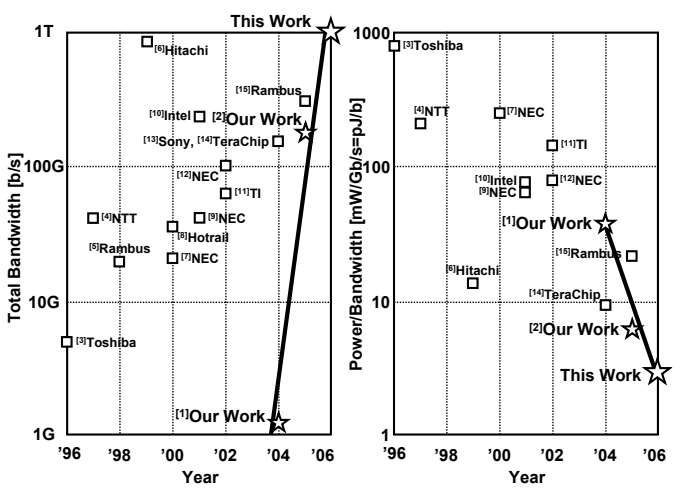

Figure 23.4.1: Transceiver chips reported at ISSCC.

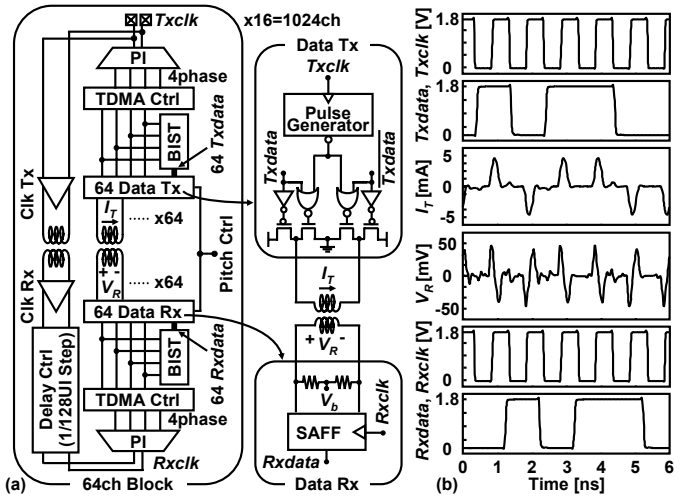

Figure 23.4.2: (a) Block diagram, (b) simulated waveforms.

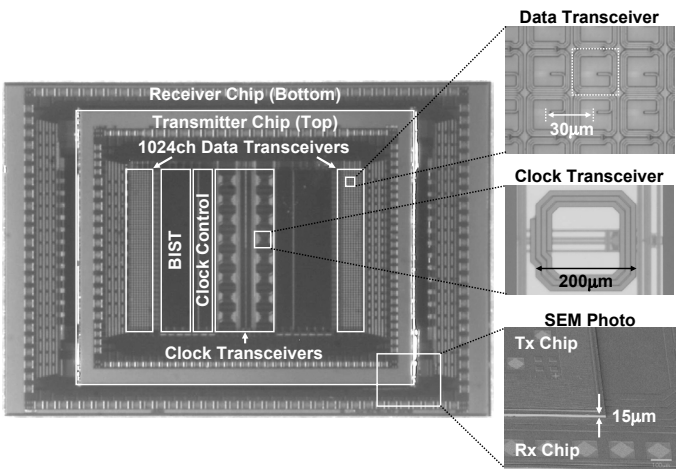

Figure 23.4.3: Micrograph of test chips. Transmitter chip is placed on top of receiver chip.

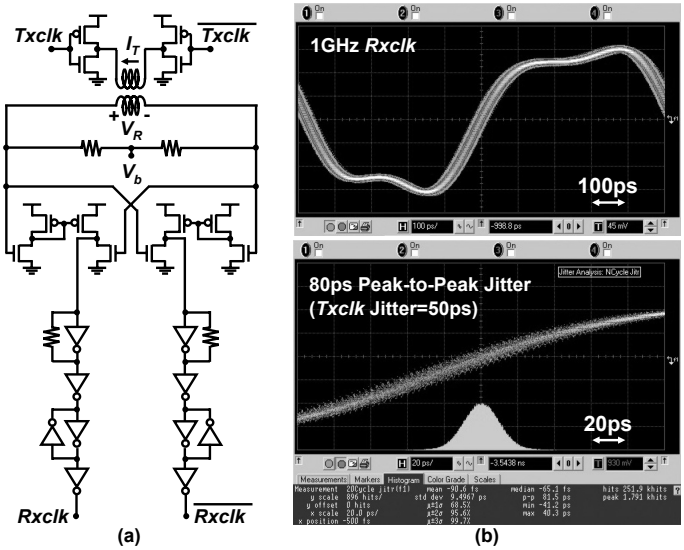

Figure 23.4.4: (a) Clock transceiver, (b) measured received clock.

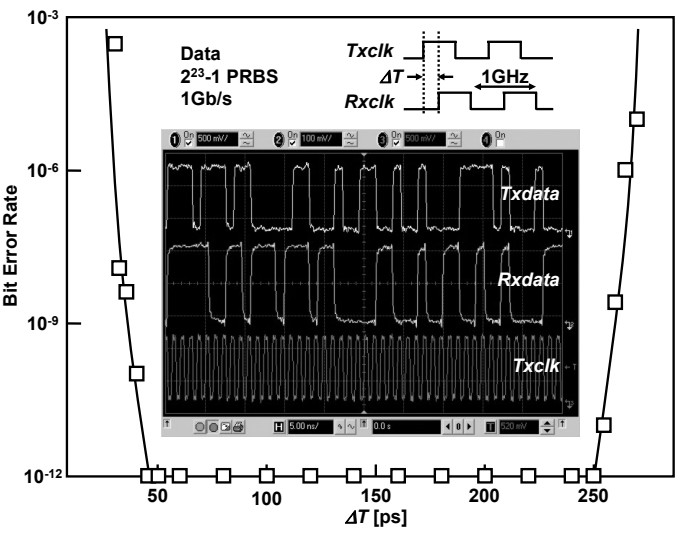

Figure 23.4.5: Measured timing bathtub curve and snapshot of data waveforms (2^{23}-1 PRBS data).

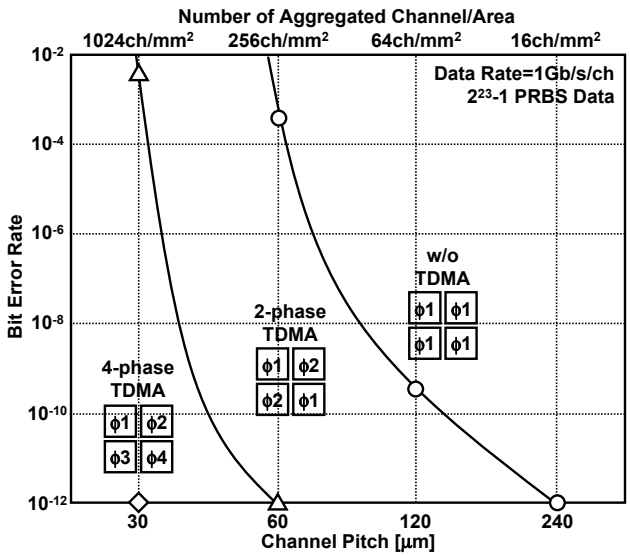

Figure 23.4.6: Measured BER dependence on channel pitch.

Continued on Page 663

Performance Summary

Total Bandwidth	1Tb/s
Number of Data Transceivers	1024
Communication Distance	15μm (Chip Thickness:10μm, Adhesive:5μm)
Power Dissipation	3W@1.8V (Tx:2.2W, Rx:0.6W, Clock:0.2W)
Total Area	2mm^2 (Data:1mm^2, Clock:1mm^2)
Channel Pitch	30μm
Process	0.18μm CMOS
Signaling	Bi-Phase Modulation + 4-phase TDMA
Clock	1GHz, Inductive Coupling

Figure 23.4.7: Performance summary.

